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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,742	01/12/2004	Gregory William Smaus	5500-90300	1112
53806	7590	03/21/2006		
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)			EXAMINER	
P.O. BOX 398			KIM, DANIEL Y	
AUSTIN, TX 78767-0398			ART UNIT	PAPER NUMBER
			2185	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/755,742

Applicant(s)

SMAUS ET AL.

Examiner

Daniel Kim

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsup (US Patent No. 7,003,629) and Beardsley et al (US Patent No. 6,345,295).

For claim 1, Alsup discloses a processor (a microprocessor, col. 1, lines 50-51) comprising:

a trace generator configured to generate a plurality of traces each including one or more operations, wherein one or more operations are decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address (a trace cache which includes several trace cache entries and a trace generator for identifying liveness groups within a trace of at least partially decoded operations, col. 1, lines 48-63); and

a trace cache memory coupled to said trace generator, wherein said trace cache memory includes a plurality of entries each configured to store one of said plurality of traces (col. 1, lines 48-63).

Despite these teachings, Alsup does not disclose the remaining claim limitations. Beardsley, however, discloses restricting each of a plurality of traces includes only

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operations having respective addresses that fall within one or more predetermined ranges of contiguous addresses (an address filter will select and conduct traces for addresses of any of the devices, and alternatively, if a number of devices have contiguous address ranges, a trace tool control may operate the address filter to select fewer address ranges, col. 4, lines 24-31).

Alsup and Beardsley are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include an address filter for restricting traces because this would allow for selecting different extents of data (col. 4, lines 57-58), as taught by Beardsley.

Claim 10 is rejected using the same rationale as for the rejection of claim 1 above.

3. Claims 2-3 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsup (US Patent No. 7,003,629), Beardsley et al (US Patent No. 6,345,295) and Cherian et al (US Patent No. 5,930,497).

For claim 2, the combined teachings of Alsup and Beardsley disclose the invention as per rejection of claim 1 above. These teachings fail, however, to disclose the limitations of claim 2.

Cherian, however, discloses a starting address of one or more predetermined ranges of contiguous addresses is based upon the respective address of a given one or more operations within a plurality of traces (an address trace is maintained for each

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process initialized by the starting address in an associated region of contiguous addresses, col. 8, lines 48-58).

Alsup, Beardsley and Cherian are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a starting address of a range of addresses to be based on trace operations because this would allow for tracking activity (col. 9, line 48), state definition, and a specification of events, conditions, outcomes (col. 8, lines 63-65), as taught by Cherian.

Claim 3 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 11 is rejected using the same rationale as for the rejections of claims 2 and 10 above.

Claim 12 is rejected using the same rationale as for the rejections of claims 3 and 10 above.

4. Claims 4-6 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsup (US Patent No. 7,003,629), Beardsley et al (US Patent No. 6,345,295), Cherian et al (US Patent No. 5,930,497) and Arsenault et al (US Patent No. 6,578,128).

For claim 4, the combined teachings of Alsup, Beardsley and Cherian disclose the invention as per the rejection of claim 2 above. These teachings fail, however, to disclose the limitations of claim 4.

Arsenault, however, discloses each of one or more predetermined ranges of contiguous addresses is separated by a predetermined number of contiguous

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addresses (a memory with a plurality of contiguous memory regions, a plurality of processors, each associated with a corresponding one of the memory regions, and each providing a plurality of sets of processor addresses, and a translator for mapping addresses fed thereto from the processors into the memory addresses, and a gap of addresses separating the last used address in a set from a first used address in a next successive set of addresses, col. 3, lines 65-67 and col. 4, lines 1-12).

Alsop, Beardsley, Cherian and Arsenault are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include ranges of contiguous addresses and a separation thereof because this allows each CPU to write into or read from its designated memory region, and only read data from appropriate memory regions (col. 8, lines 62-66), as taught by Arsenault.

Claim 5 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 6 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 13 is rejected using the same rationale as for the rejections of claims 4 and 11 above.

Claim 14 is rejected using the same rationale as for the rejections of claims 5 and 11 above.

Claim 15 is rejected using the same rationale as for the rejections of claims 6 and 11 above.

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5. Claims 7-9 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsup (US Patent No. 7,003,629), Beardsley et al (US Patent No. 6,345,295) and Hughes (US Patent No. 6,973,543).

For claim 7, the combined teachings of Alsup and Beardsley disclose the invention as per rejection of claim 1 above. These teachings fail, however, to disclose the limitations of claim 7.

Hughes, however, discloses a trace cache control unit coupled to said trace cache memory and configured to receive a trace cache probe and to store in a trace cache probe storage, an address corresponding to said trace cache probe until said trace cache probe completes (a memory configured to store an indication of one or more addresses, wherein the memory is coupled to receive a first address of a read command, and a control circuit coupled to the memory is configured to cause an issuance of one or more probes corresponding to the read command responsive to the first address missing in the memory, and inhibit the issuance of one or more probes corresponding to the read command responsive to the first address hitting in the memory, col. 2, lines 17-26).

Alsup, Beardsley and Hughes are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a trace cache probe and storage thereof because this would maintain coherency of cache data (col. 2, line 10), and by inhibiting probes appropriately, system bandwidth which

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would be consumed by the probes may be conserved (col. 1, lines 66-67), as taught by Hughes.

Claim 8 is rejected using the same rationale as for the rejection of claim 7 above.

Claim 9 is rejected using the same rationale as for the rejection of claim 7 above.

Claim 16 is rejected using the same rationale as for the rejections of claims 7 and 10 above.

Claim 17 is rejected using the same rationale as for the rejections of claims 8 and 16 above.

Claim 18 is rejected using the same rationale as for the rejections of claims 9 and 17 above.

Citation of Pertinent Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Groeschel (US PGPub No. 20040216091) discloses memory allocation trace data is analyzed by generating a sorted address index containing records of memory allocations, deallocations, and memory address inquiries.

Bala (US Patent No. 6,233,678) discloses collecting a branch history value of a program executing in a processor, and a current start address register latches a program count value in response to a trace termination condition.

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Ayers (US Patent No. 5,210,843) discloses a pseudo set-associative memory caching arrangement with a plurality of cache memory banks each comprising a respective number of addressable locations individually defined by a cache address.

Contact Information

7. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

3-15-06

Pierre Vital
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PRIMARY EXAMINER